UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/591,226	06/09/2000	David Robert Baldwin	TD-156	3469

7590 06/04/2003

Robert Groover (Patent Docketing)
Arter & Hadden LLP
1100 Huntington Bldg
925 Euclid Ave
Cleveland, OH 44115

EXAMINER
TUNG, KEE M

ART UNIT	PAPER NUMBER
2676	9

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/591,226	BALDWIN, DAVID ROBERT	
	Examiner	Art Unit	
	Kee M Tung	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

The amendment filed 4/28/03 has been considered in preparing this Office action.

As per claims 2 and 3, line 4, "said chip" is not clear as which chip is being referred to, a graphics processing chip (line 1) or a graphics accelerator chip (line 2).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peddada et al (6,295,068) in view of Porterfield (6,249,853).

Peddada teaches a graphics processing method (Figs. 4-6) comprising performing 3D graphics rendering in a graphics accelerator subsystem (Fig. 5, 20), using a dedicated graphics memory (22 and 24) as primary memory for rendering accelerator logic; using a system main memory (14) as additional memory to hold textures required by said rendering accelerator logic; and when textures required by sad rendering accelerator logic are not present in said dedicated graphics memory, then either downloading said textures from main memory into said graphics memory (Fig. 5, can be download from disk 18 to AGP mem 14 to texture cache 24). However, Peddada fails to explicitly suggest or teach, selectively, when commanded by a software application, allowing said accelerator logic to read textures directly from said

main memory without downloading them into said graphics memory. Peddada teaches there are two AGP models. One is known as the AGP DMA model which downloading texture data from main memory into texture cache in the graphics accelerator (col. 1, line 63 through col. 2, line 9) and another is known as AGP Execute model, has 3D graphics accelerator accessing textures from AGP memory (part of the main memory) via system logic chip over AGP bus (col. 1, lines 50-57). However, Peddada uses a different way to achieve the benefit of AGP Execute model. Porterfield also teaches two AGP models, a DMA and Execute models (col. 6, line 55 through col. 7, line 5). Porterfield teaches an AGP Execute model by add additional mapping mechanism, such as, GART which is also known to Peddada (col. 1, lines 58-62 and col. 9, lines 6-32). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Porterfield into Peddada in order to use both AGP models and thus to add the flexibility to the system. Therefore, at least claim 1 would have been obvious.

As per claim 4, Porterfield teaches said accelerator logic is able to read non-contiguous textures directly from said main memory (col. 6, line 65 to col. 7, line 5).

3. Claims 2, 3, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Porterfield (6,249,853) in view of Mergard et al (5,941,968) or Poirion (6,232,990) or Chen et al (6,292,201).

Porterfield teaches a graphics processing chip (Fig. 3, 160) comprising rendering acceleration chip (part of the graphics accelerator 160); and software which has a user accessible mechanism in place to do logical-to-physical mapping into a main system

memory (MMU portion of the system logic 154, i.e., the same logic for both Fig. 1 and 3, and further see col. 6, lines 22-32 and col. 6, line 55 through col. 8, line 3 and Figs. 4 and 5a). However, Porterfield fails to explicitly suggest or teach the software integrated on the chip with the graphics accelerator chip. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of Porterfield into a single chip integrated circuit in order to achieve a low cost, low space system without sacrificing overall performance. All three of Mergard et al, Poirion or Chen teaches a single chip integrated circuit that combines the graphics accelerator and system logic plus many other system components into a single chip integrated circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Mergard et al, Poirion or Chen into the system of Porterfield in order to provide a single chip integrated circuit as claimed in order to achieve the different advantages as taught by Mergard et al (abstract), Poirion (col. 2, line 4 through col. 3, line 17) or Chen (col. 3, line 35 through col. 4, line 30). Therefore, at least claim 2 would have been obvious.

As per claim 5, Porterfield teaches the software is able to read noncontiguous textures directly from said main memory (col. 7, lines 21-31).

Claim 3 is similar in scope to claim 2, and additionally requires a texture memory management function, integrated on said chip, which manages both texture storage in host memory and also texture storage in normal texture memory (part of the function of the graphics accelerator, col. 6, lines 55-61).

As per claim 6, Porterfield teaches said texture memory management function is able to read noncontiguous texture directly from said main memory (col. 6, lines 61-67).

4. Claims 2, 3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peddada et al (6,295,068) in view of Mergard et al (5,941,968) or Poirion (6,232,990) or Chen et al (6,292,201).

Peddada et al teaches a graphics processing chip (Fig. 5, 20) comprising rendering acceleration chip (part of the graphics accelerator 20); and software which has a user accessible mechanism in place to do logical-to-physical mapping into a main system memory (cache management process, col. 4, lines 4-12). However, Peddada et al fails to explicitly suggest or teach the software integrated on the chip with the graphics accelerator chip. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of Peddada et al into a single chip integrated circuit in order to achieve a low cost, low space system without sacrificing overall performance. All three of Mergard et al, Poirion or Chen teaches a single chip integrated circuit that combines the graphics accelerator and system logic plus many other system components into a single chip integrated circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Mergard et al, Poirion or Chen into the system of Peddada et al in order to provide a single chip integrated circuit as claimed in order to achieve the different advantages as taught by Mergard et al (abstract), Poirion (col. 2, line 4 through col. 3, line 17) or Chen (col. 3, line 35 through col. 4, line 30). Therefore, at least claim 2 would have been obvious.

As per claim 5, Peddada teaches the software is able to read noncontiguous textures directly from said main memory (col. 9, lines 20-31).

Claim 3 is similar in scope to claim 2, and additionally requires a texture memory management function, integrated on said chip, which manages both texture storage in host memory and also texture storage in normal texture memory (part of the function of the graphics accelerator 20 to access both memories).

As per claim 6, Porterfield teaches said texture memory management function is able to read noncontiguous texture directly from said main memory (col. 9, lines 20-31).

Response to Arguments

5. Applicant's arguments filed 4/28/03 have been fully considered but they are not persuasive.

Regarding claim 1, applicant argues that none of the references of record meet the claim 1's recitation of "either downloading said textures .... or selectively, when commanded ... into said graphics memory." The examiner disagrees. The combined system clearly suggests or teaches the claimed feature. For example, Peddada teaches downloading said texture to texture cache 50 (Fig. 5) and Porterfield teaches, in addition to DMA model, "the graphics accelerator of the present invention can also use, or "execute," graphics data directly from main memory" (col. 6, lines 61-67).

Regarding claim 2, applicant argues that none of the prior art shows "software, integrated on said chip, which has a user accessible mechanism in place to do logical-to-physical mapping into a main system memory." Well, the examiner disagrees

because the combined system suggests the claimed subject matter, one teaches off-chip software logical-to-physical mapping and the other suggests to incorporate the off-chip software can be incorporated into on-chip as detailed above.

Regarding two AGP modes, applicant argues "there is no teachings in the art of record which suggests combining them at all." This is not trued. Porterfield clearly suggests the two modes, "in contrast to DMA model ... the graphics accelerator of the present invention **can also** use, "**execute**," graphics data **directly** from the memory in which it resides." (col. 6, lines 61-67).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kee M Tung whose telephone number is 703-305-9660. The examiner can normally be reached on Tuesday - Friday from 6:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

kmt
June 3, 2003

Kee M Tung
Primary Examiner
Art Unit 2676